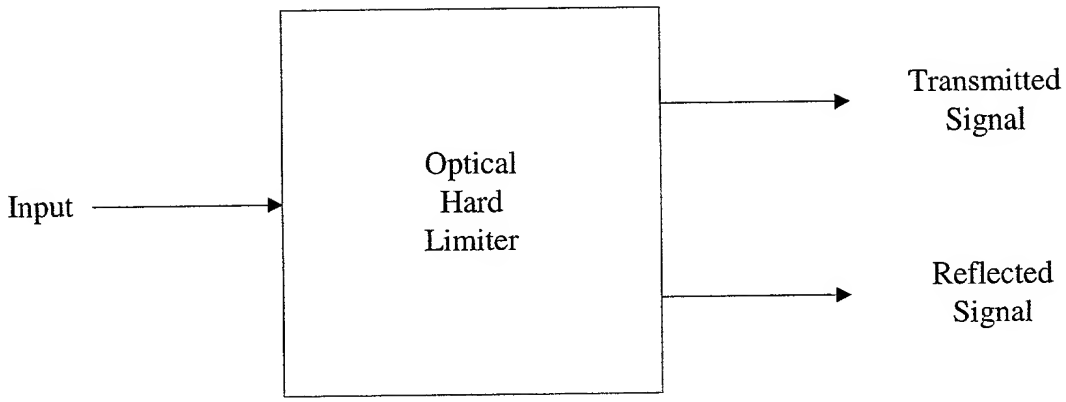

FIG. 1 100

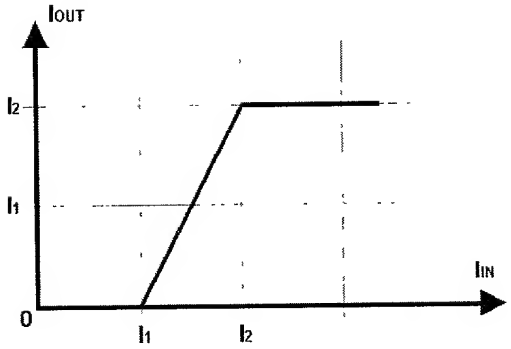

FIG. 2A 200

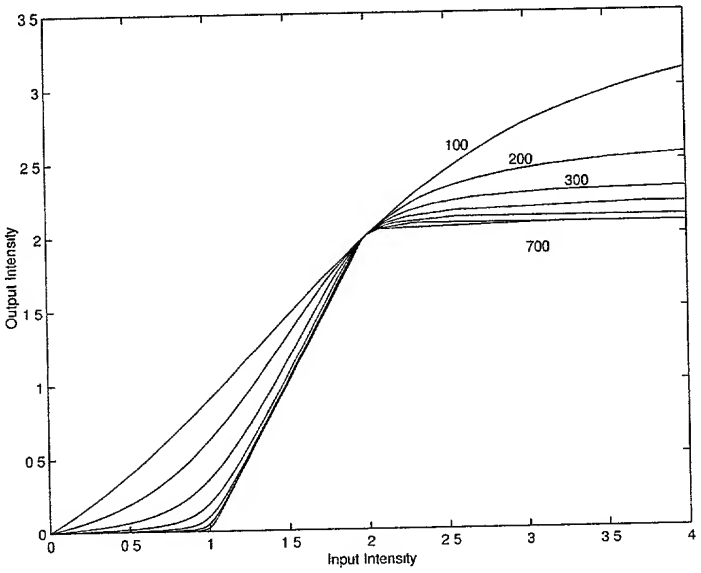

FIG. 2B 210

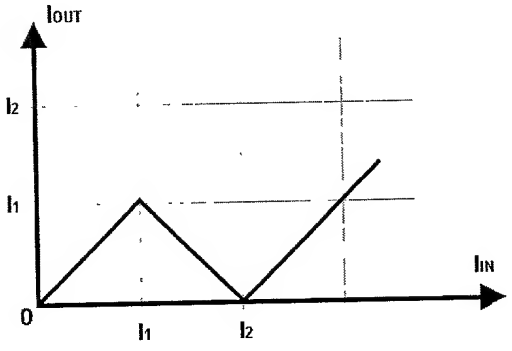

FIG. 3 300

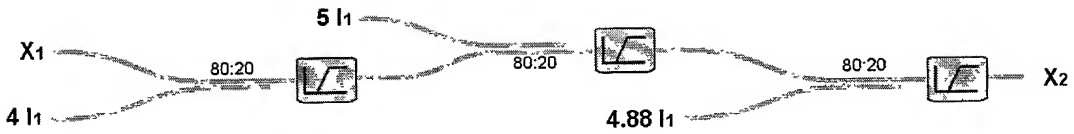

FIG. 4 400

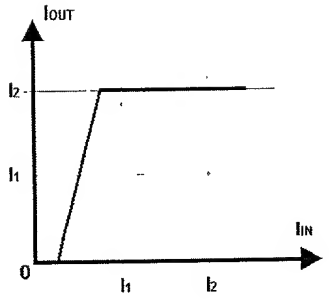

FIG. 5 500

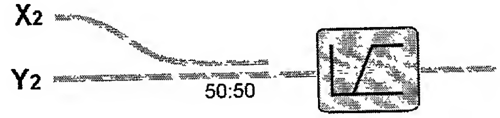

FIG. 6 <u>600</u>

FIG. 7 <u>700</u>

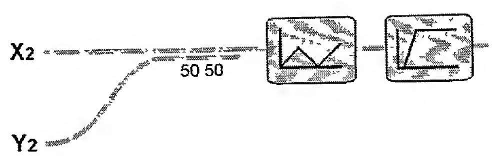

FIG. 8 <u>800</u>

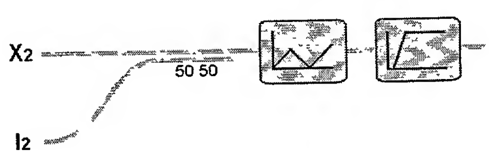

FIG. 9 <u>900</u>

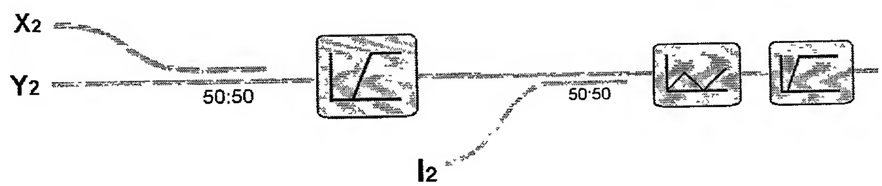

FIG. 10 1000

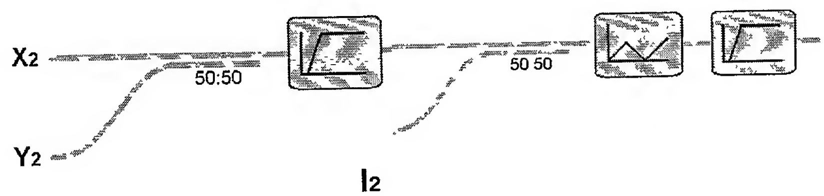

FIG. 11 1100

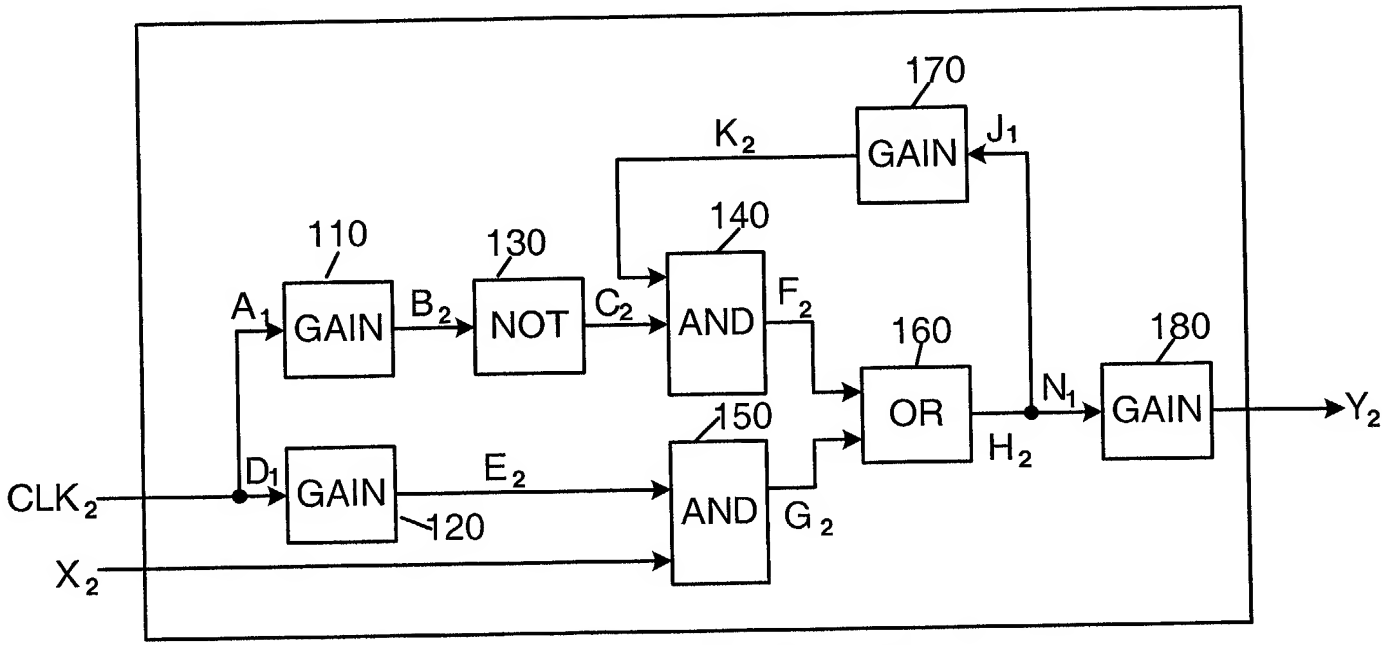
170
K2
GAIN
J1
140
110
130
A1
GAIN
B2
NOT
C2
AND
F2
160
180
OR
N1
GAIN
Y2
150
CLK2
D1
GAIN
E2
AND
G2
120
X2

FIG. 12 1200

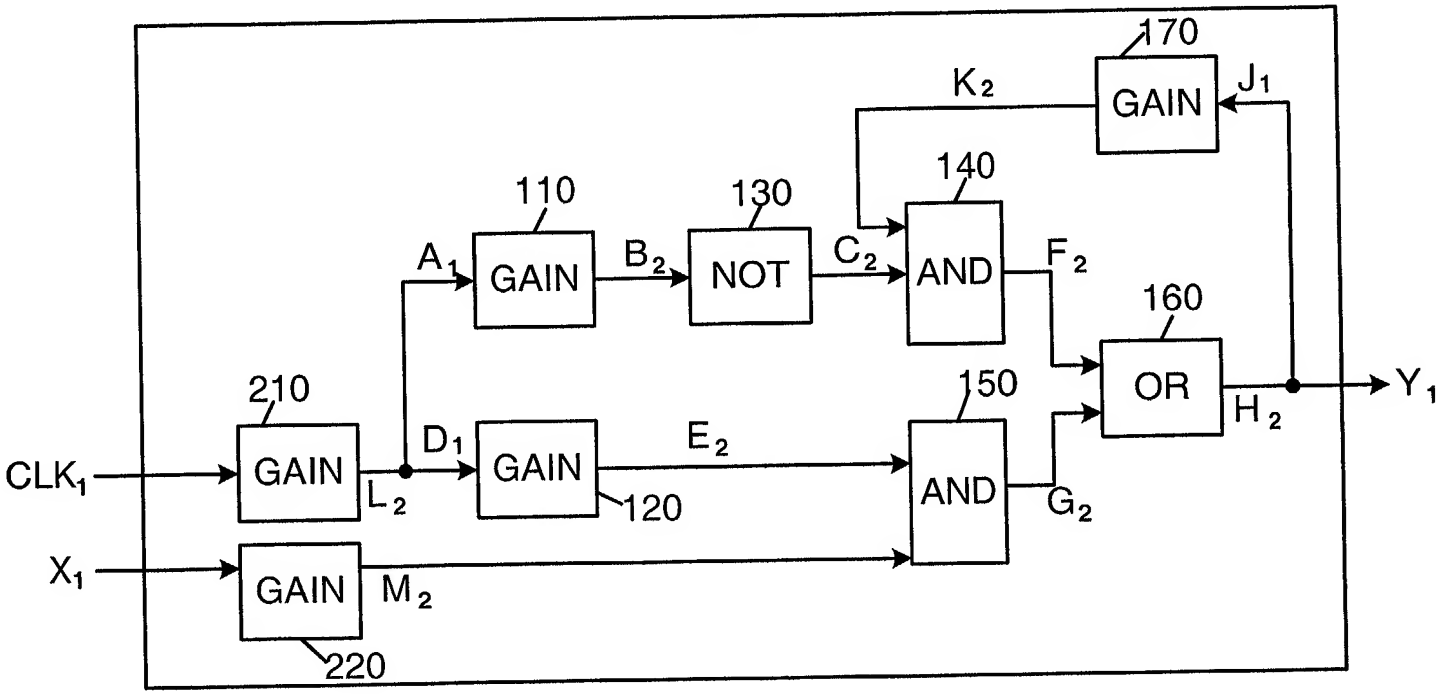
170
K2
GAIN
J1
140
110
130
A1
GAIN
B2
NOT
C2
AND
F2
160
OR
Y1
H2
210
150
CLK1
GAIN
L2
D1
GAIN
E2
120
AND
G2
X1
GAIN
M2
220

FIG. 13 1300

	0 < INPUT < I1	I1 < INPUT < I2	I2 < INPUT
ITRANSMITTED	0	2*INPUT - I2	I2
IREFLECTED	INPUT	I2 - INPUT	INPUT - I2

FIG. 14 <u>1400</u>

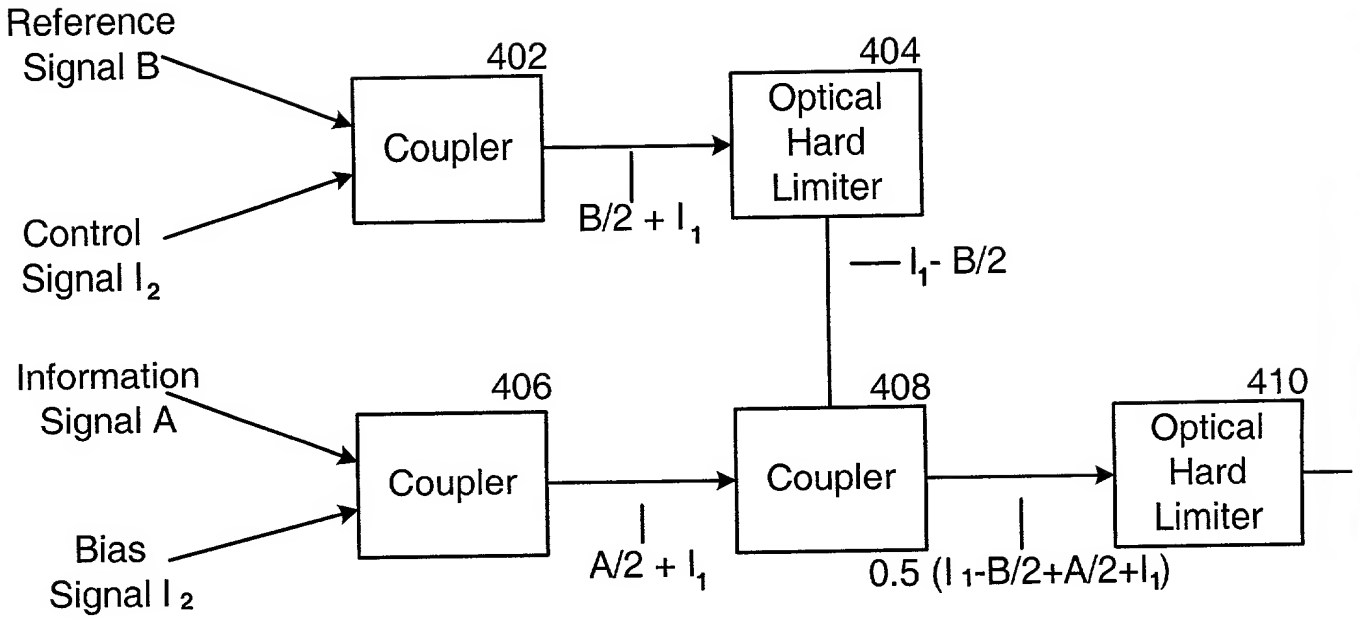

FIG. 15 1500

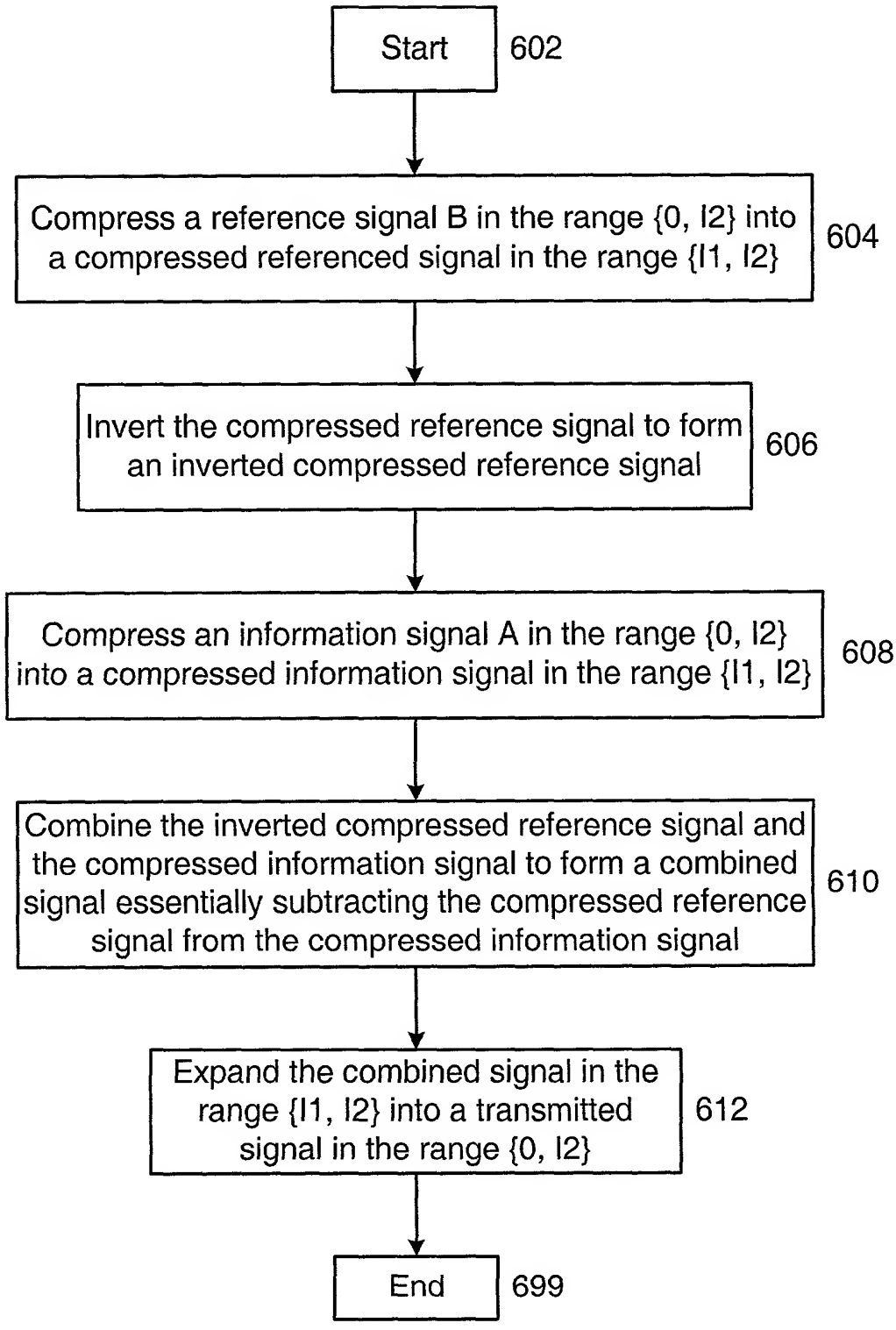
Start
602
Compress a reference signal B in the range {0, I2} into a compressed referenced signal in the range {I1, I2}
604
Invert the compressed reference signal to form an inverted compressed reference signal
606
Compress an information signal A in the range {0, I2} into a compressed information signal in the range {I1, I2}
608
Combine the inverted compressed reference signal and the compressed information signal to form a combined signal essentially subtracting the compressed reference signal from the compressed information signal
610
Expand the combined signal in the range {I1, I2} into a transmitted signal in the range {0, I2}
612
End
699

FIG. 16 1600

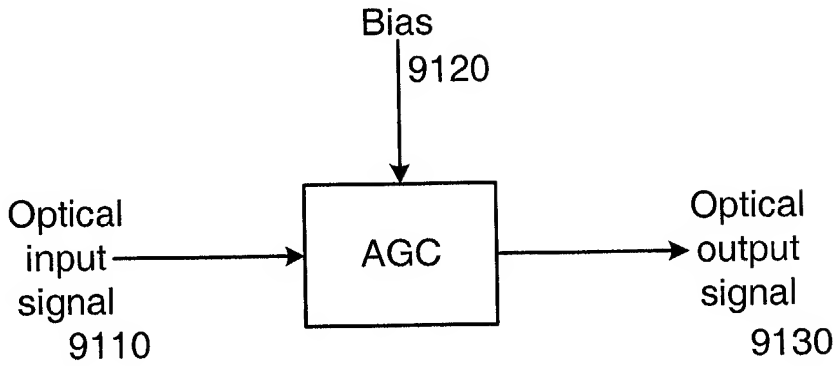
Bias
9120
Optical
input
signal
9110
AGC
Optical
output
signal
9130

FIG. 17 9100

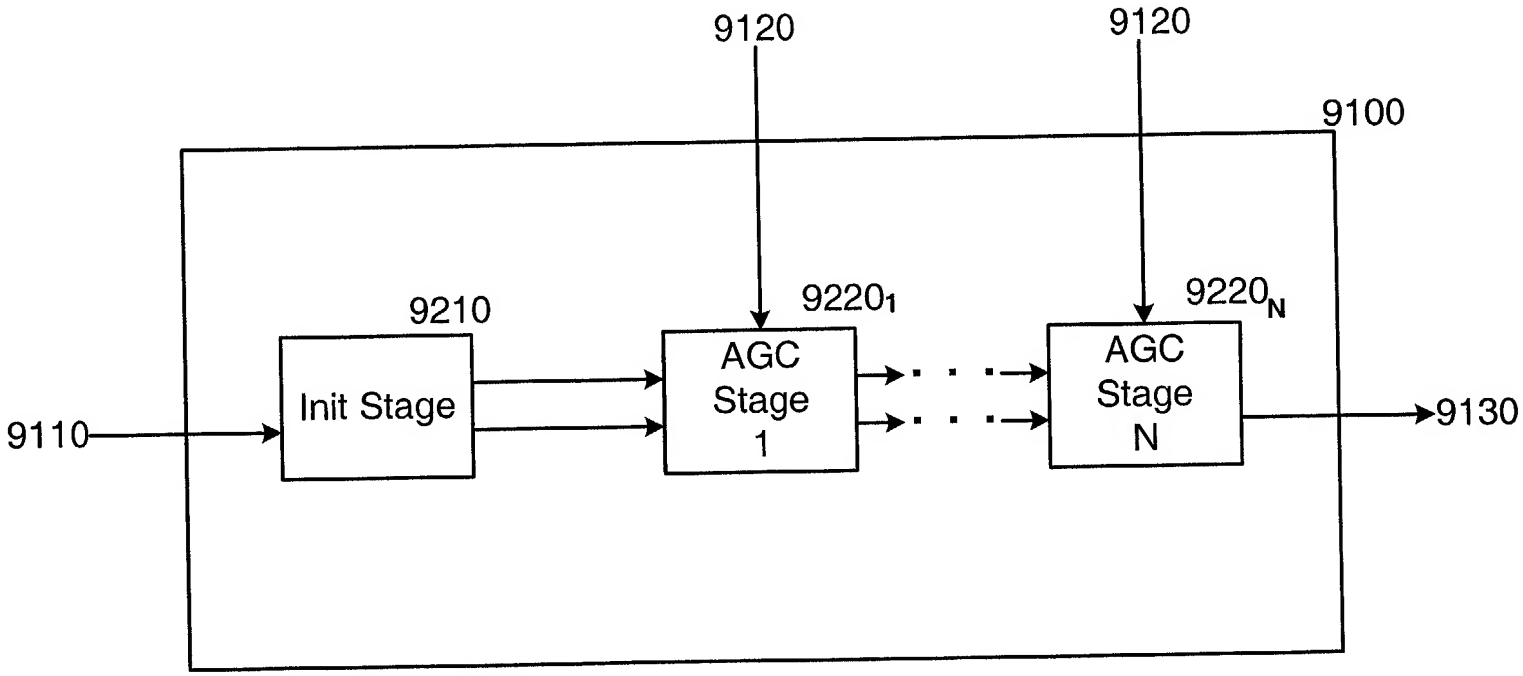

FIG. 18

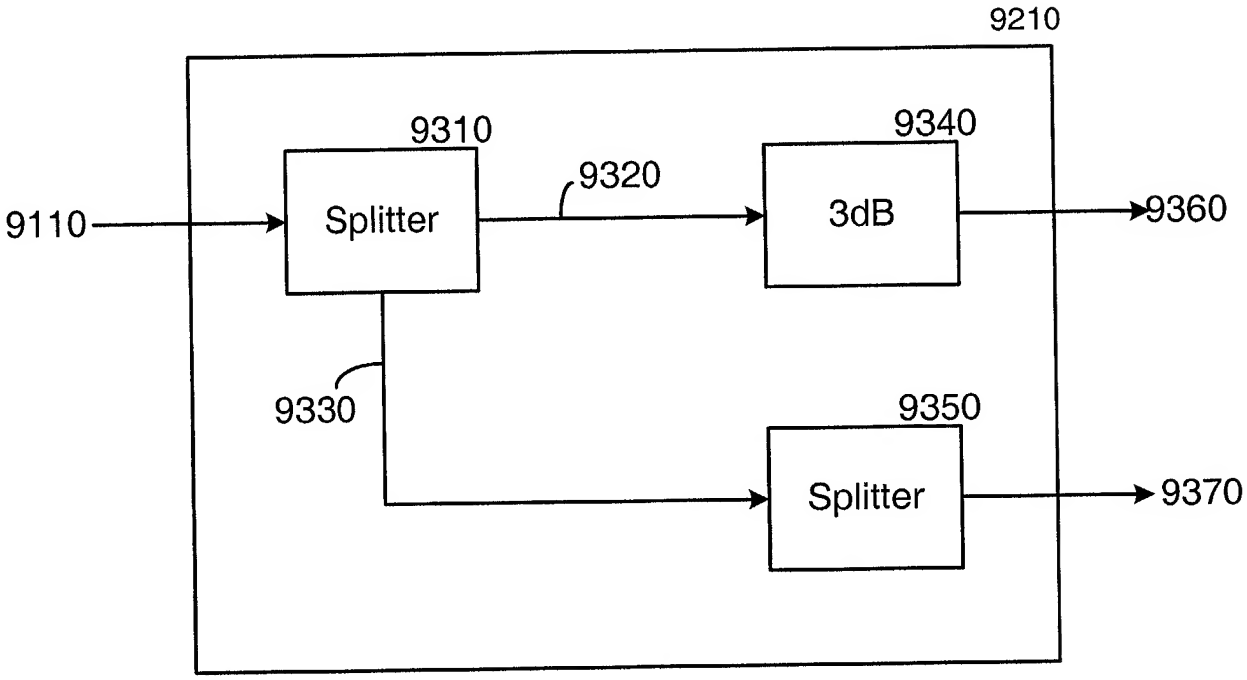
9210
9310
9340
9320
9110
Splitter
3dB
9360
9330
9350
Splitter
9370

FIG. 19

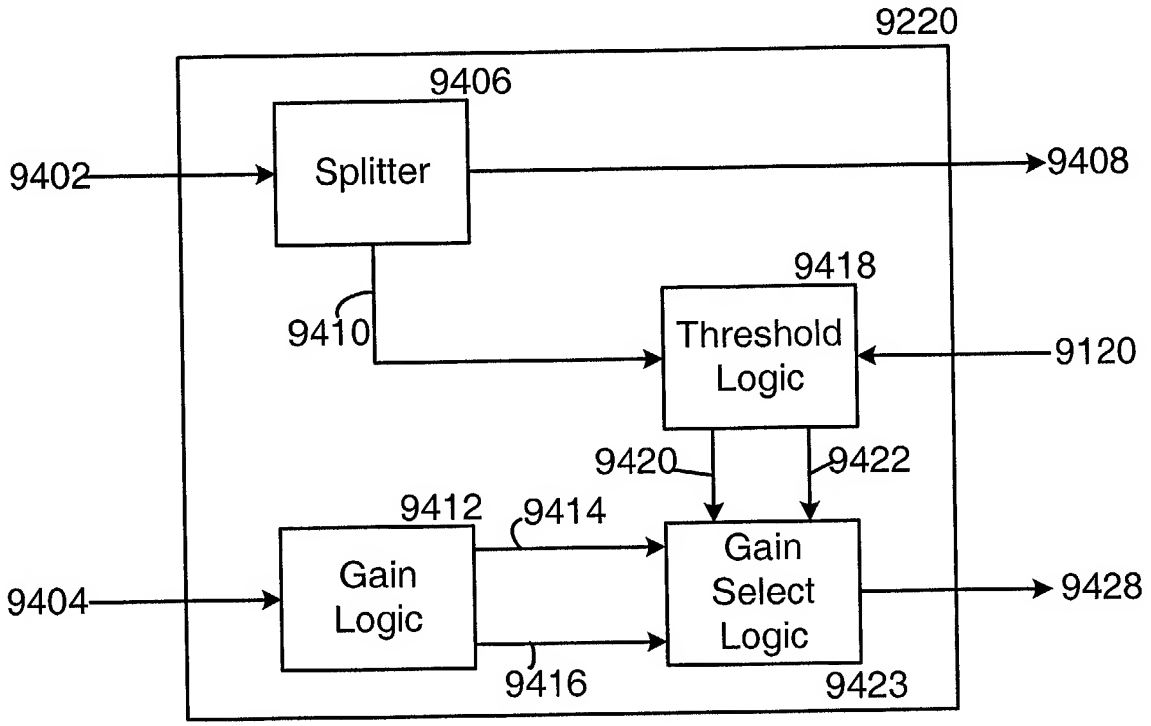
9220
9406
9402
Splitter
9408
9418
9410
Threshold Logic
9120
9420
9422
9412
9414
Gain Logic
Gain Select Logic
9404
9428
9416
9423

FIG. 20

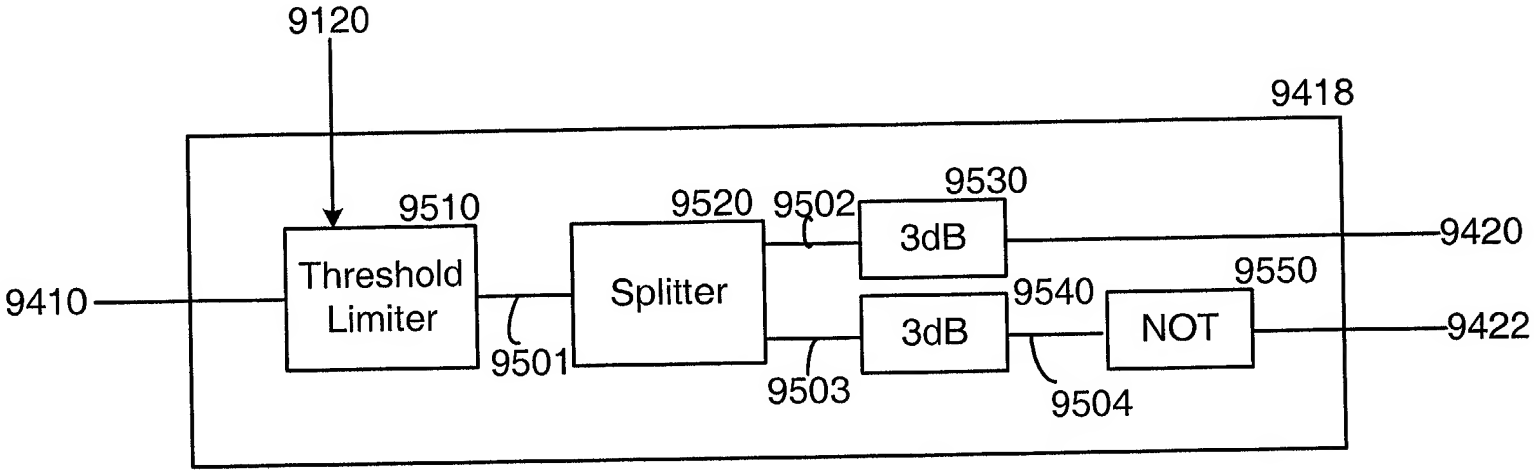

FIG. 21

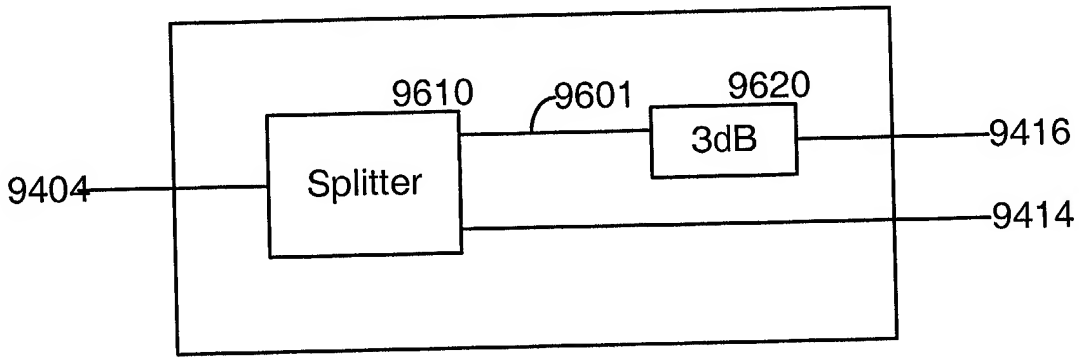

FIG. 22

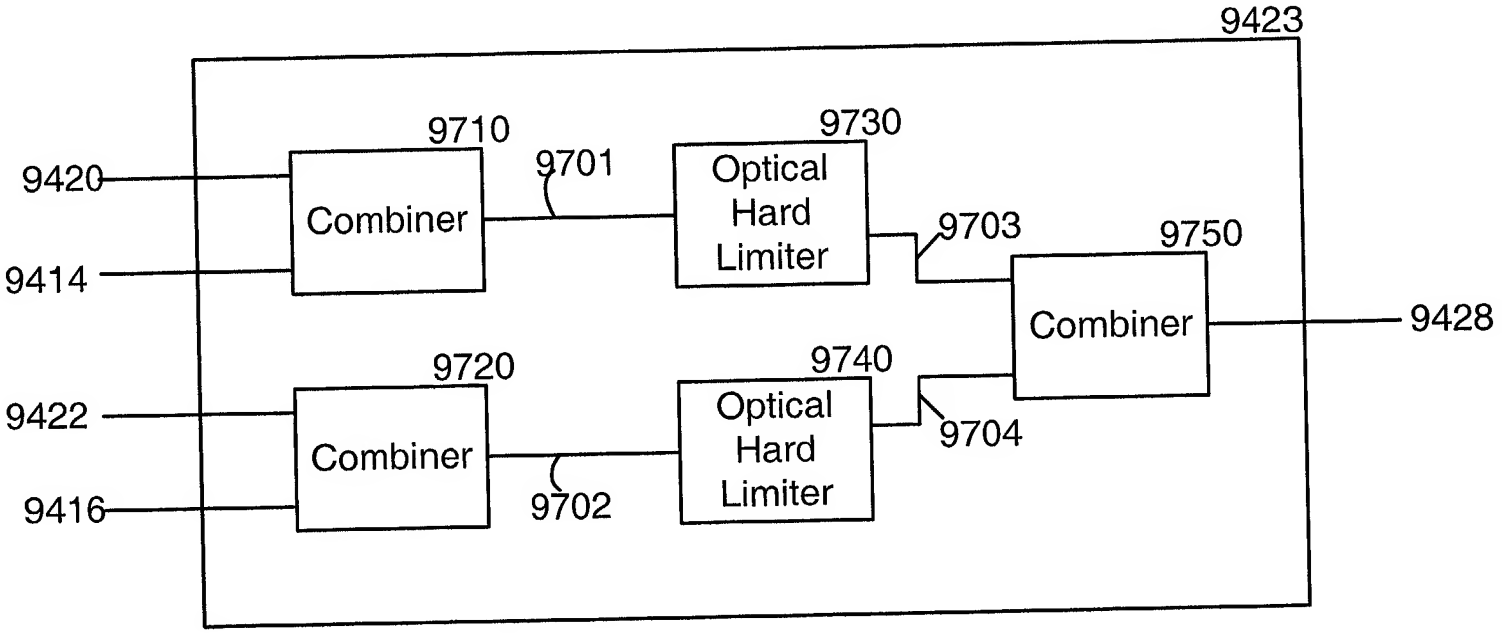
9423
9710
9730
9420
Combiner
9701
Optical
Hard
Limiter
9703
9750
9414
Combiner
9428
9720
9740
9422
Combiner
Optical
Hard
Limiter
9704
9416
9702

FIG. 23

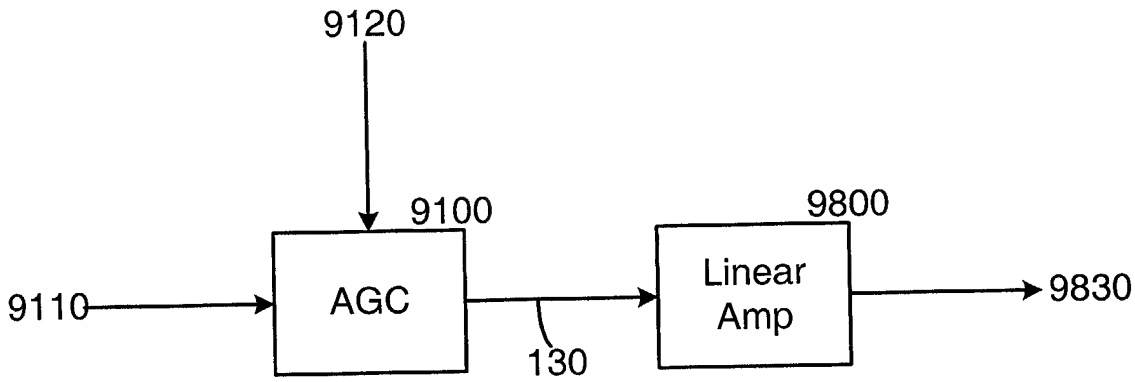

FIG. 24

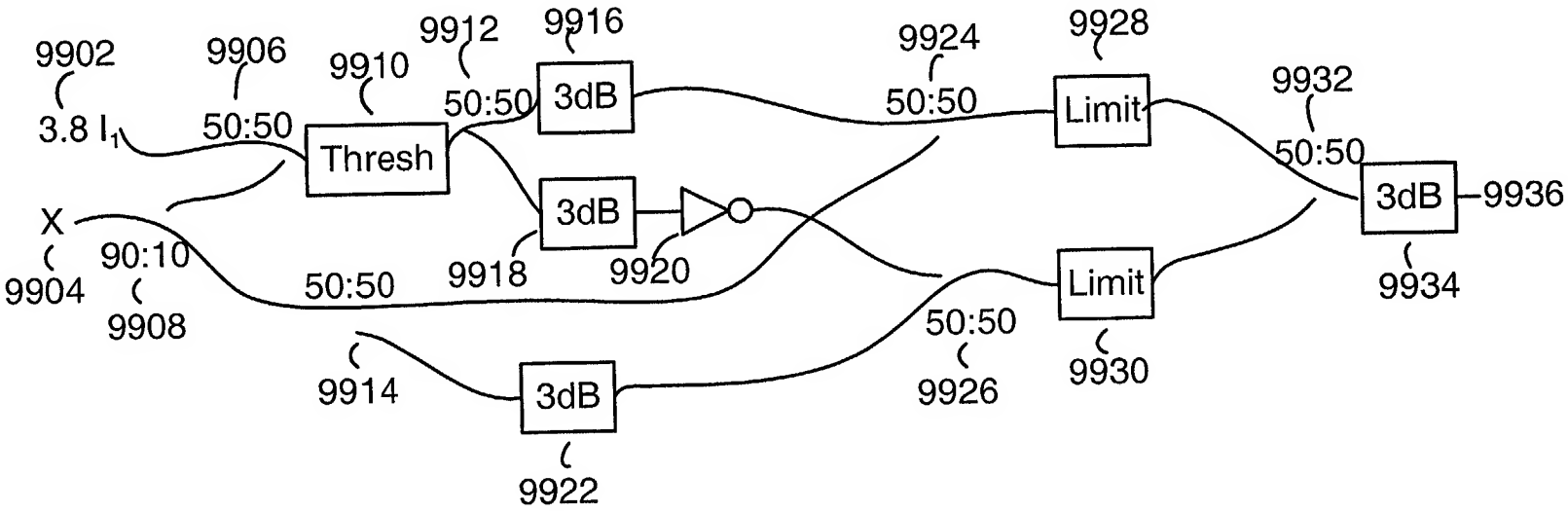

FIG. 25 9900

data bits							address bits					flag
D	D	D	D	D	D	D	N	N-1	• • •	2	1	F

FIG. 26 8100

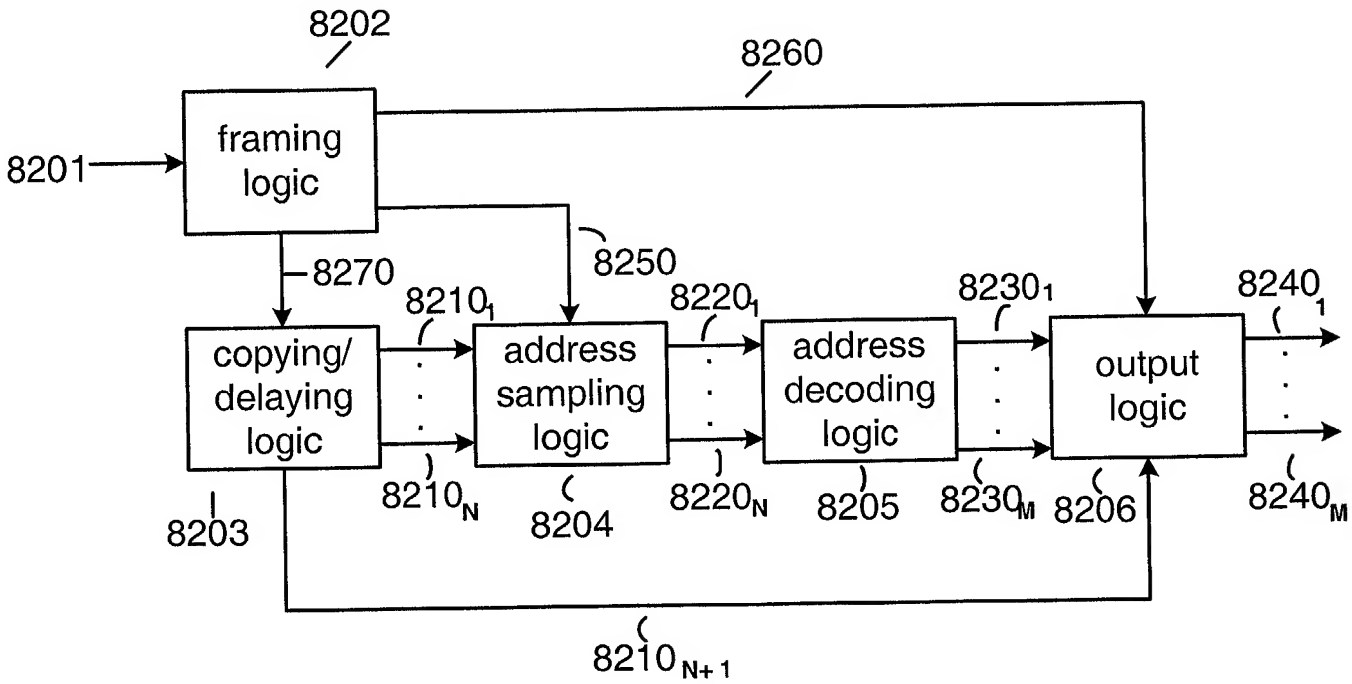

FIG. 27 8200

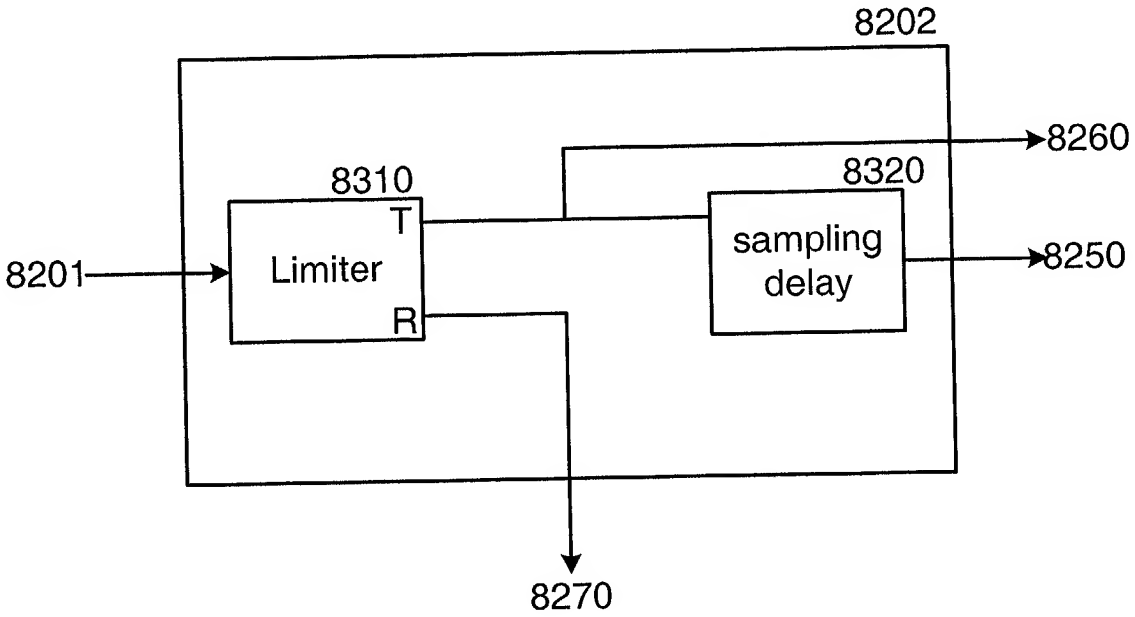
8202
8260
8310
8320
T
Limiter
sampling
delay
8201
8250
R
8270

FIG. 28

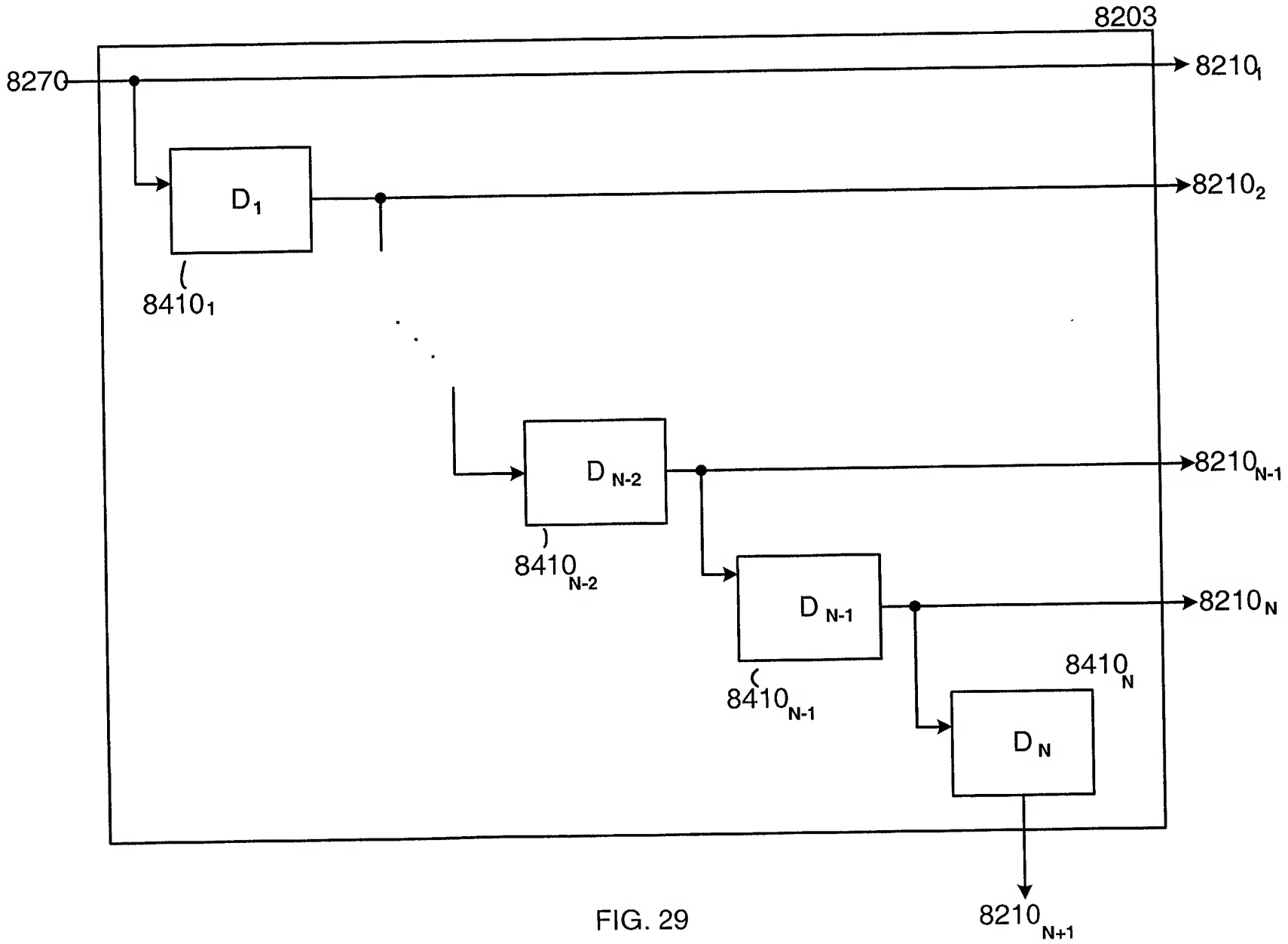

FIG. 29

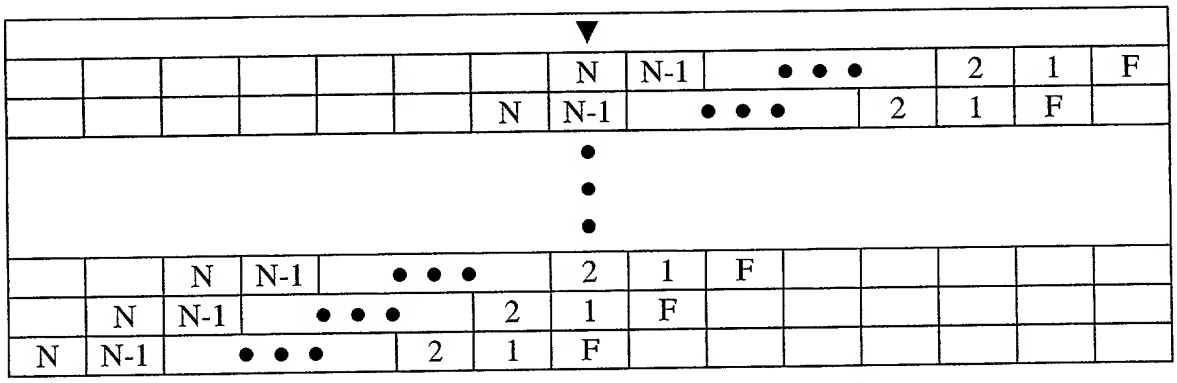

FIG. 30

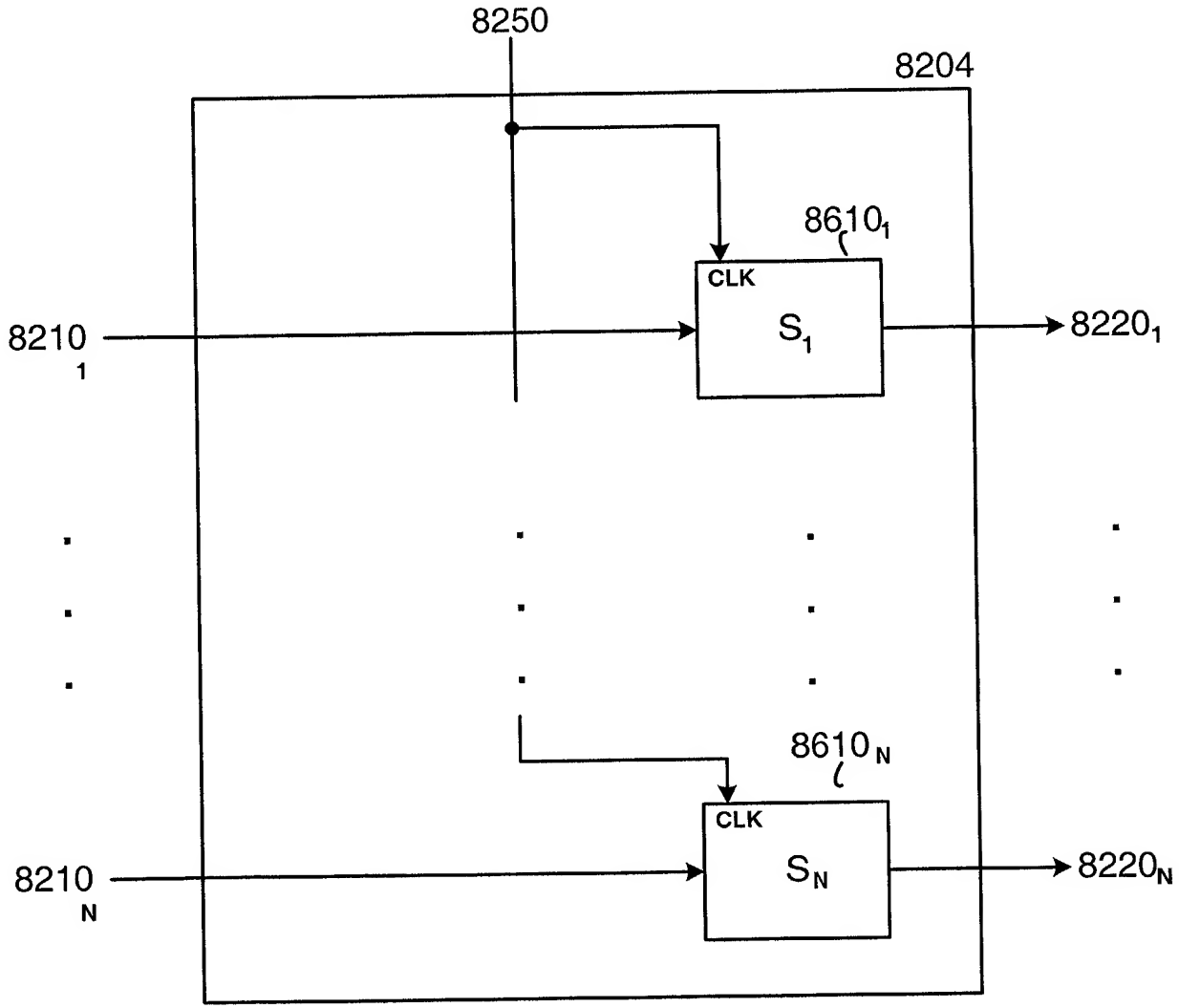

FIG. 31

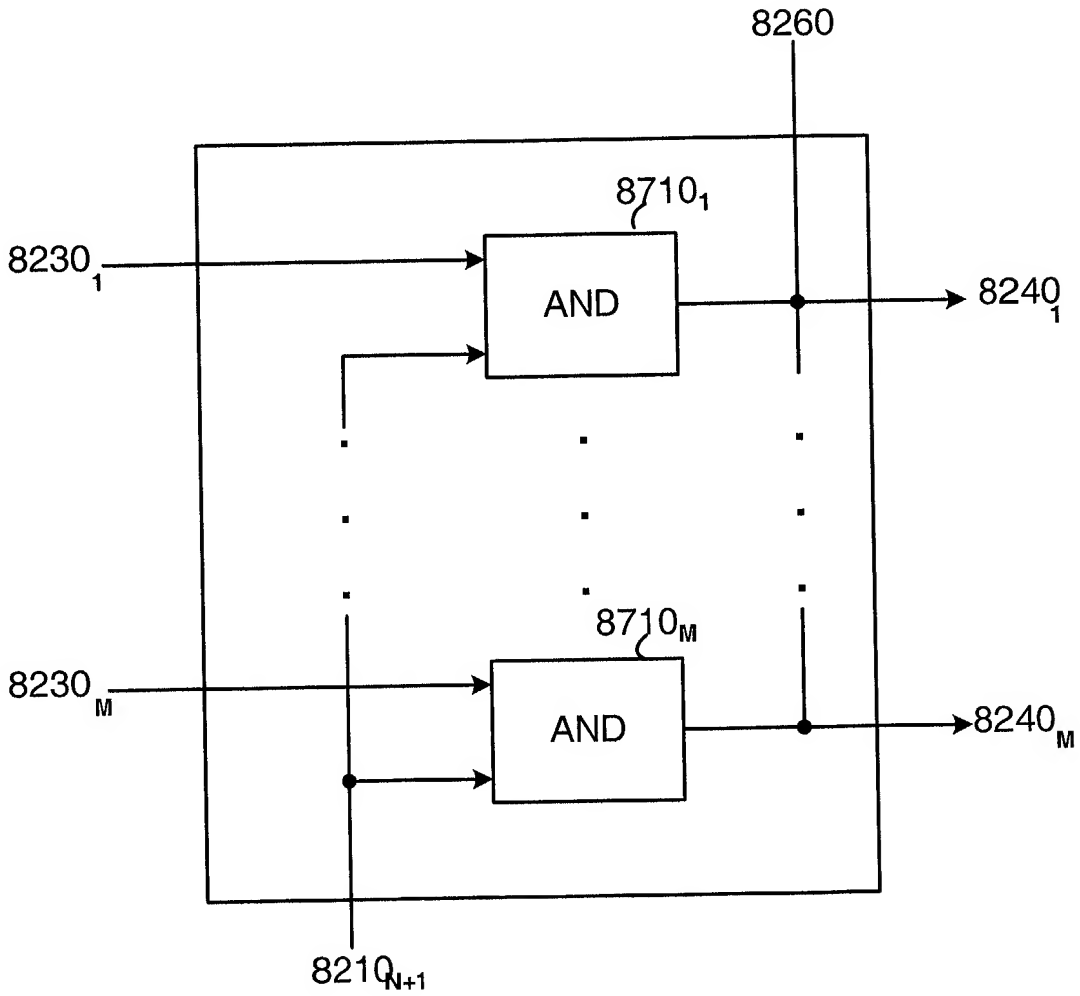

FIG. 32

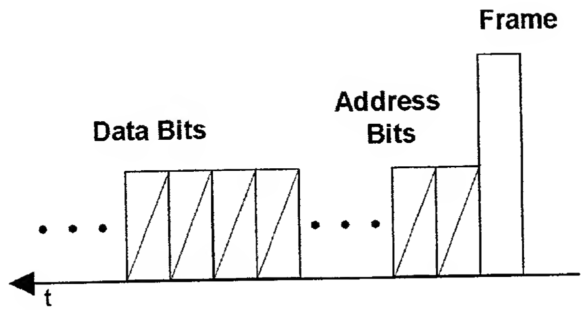

FIG. 33 8800

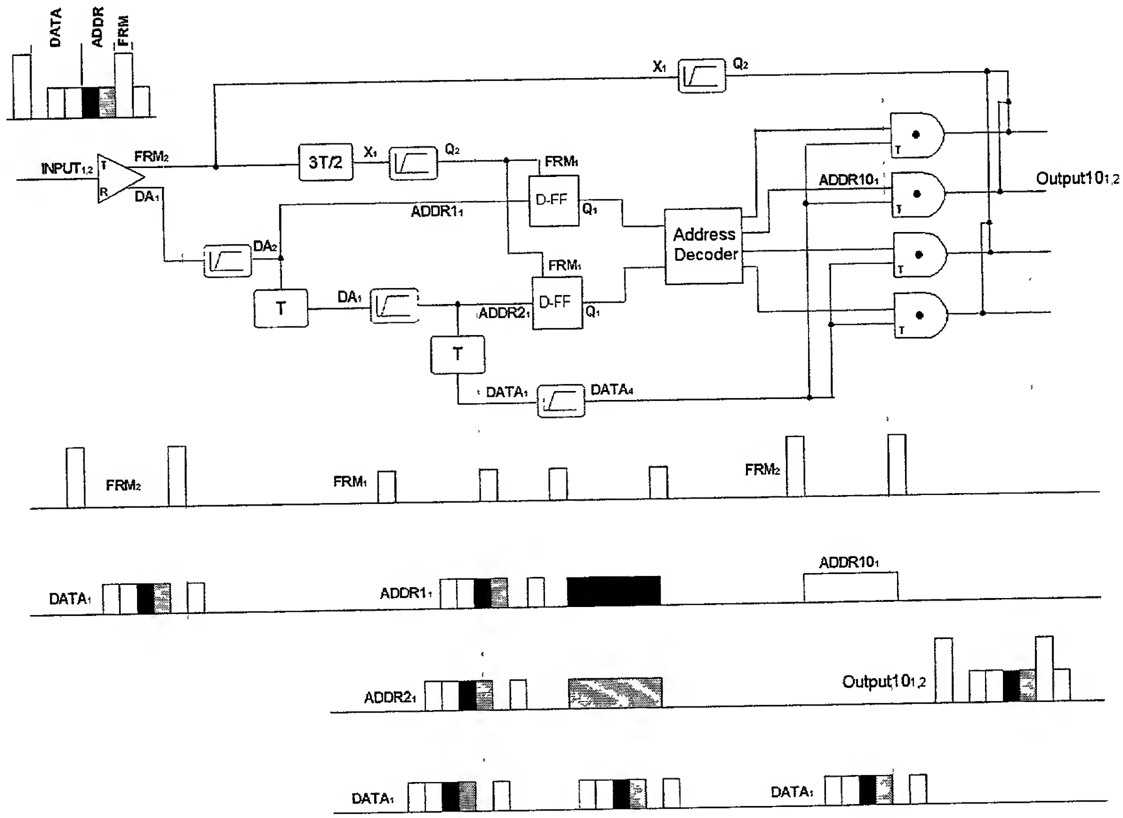
DATA
ADDR
FRM
INPUT1,2
FRM2
DA1
3T/2
X1
Q2
FRM1
D-FF
Q1
ADDR11
DA2
T
ADDR21
DATA1
DATA4
Address Decoder
ADDR101
Output101,2
FRM2
FRM1
DATA1
ADDR11
ADDR101
ADDR21
Output101,2
DATA1

FIG. 34 8900

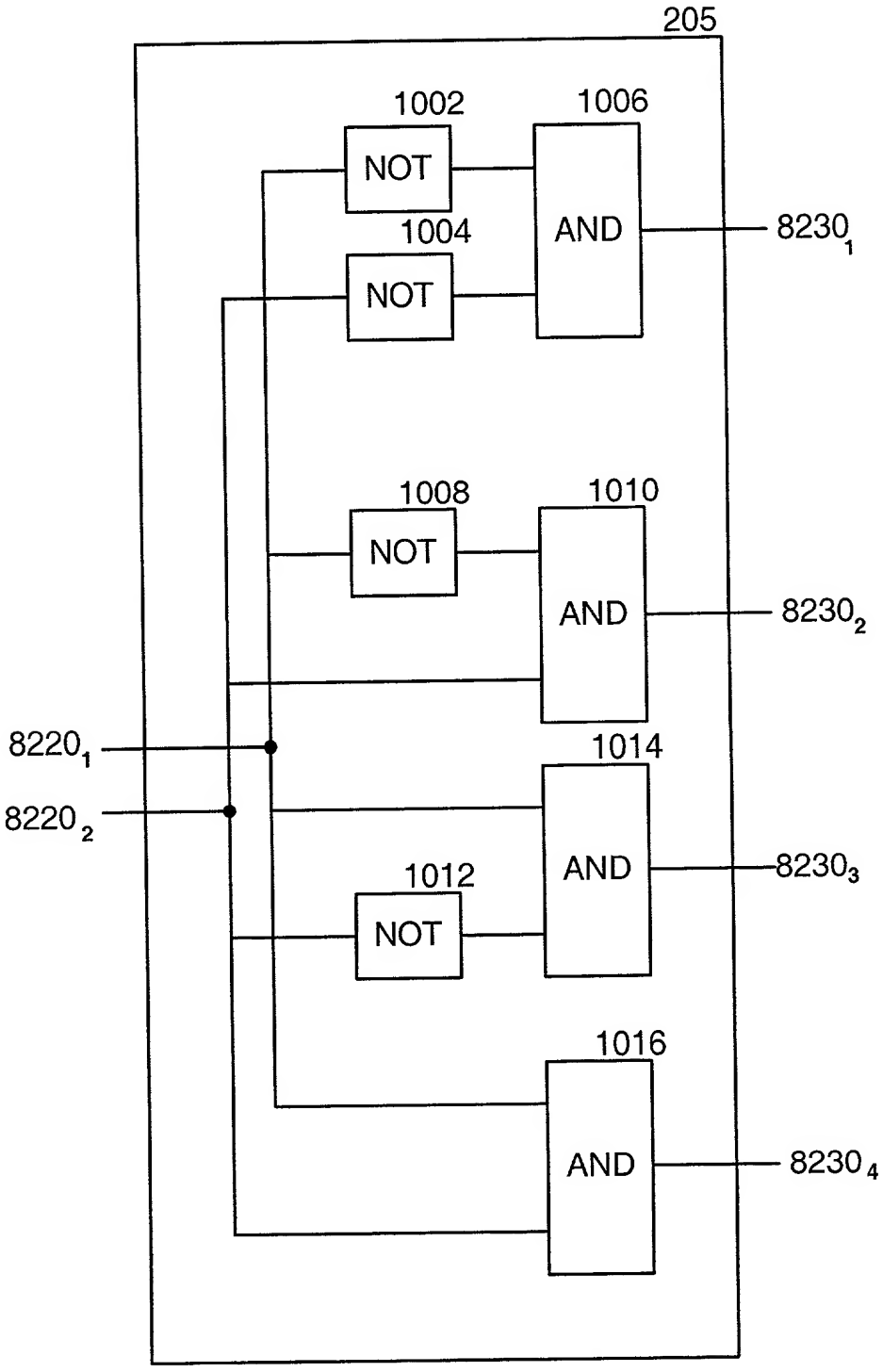
205
1002
1006
NOT
AND
8230 1
1004
NOT
1008
1010
NOT
AND
8230 2
8220 1
1014
8220 2
AND
8230 3
1012
NOT
1016
AND
8230 4

FIG. 35

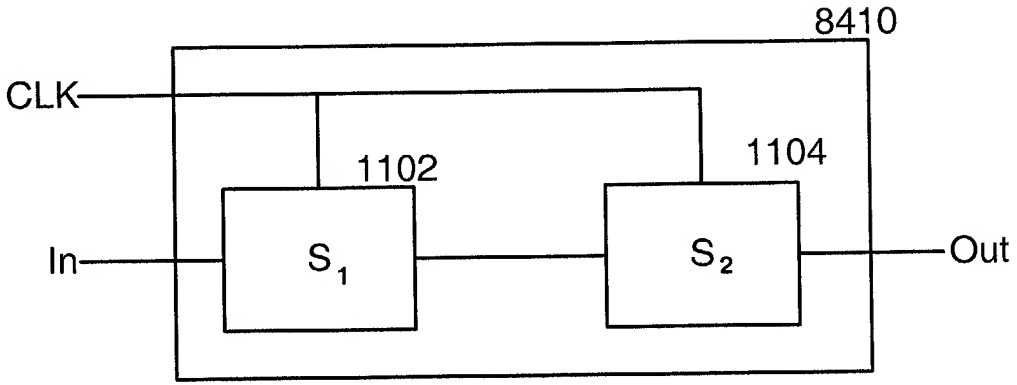

FIG. 36

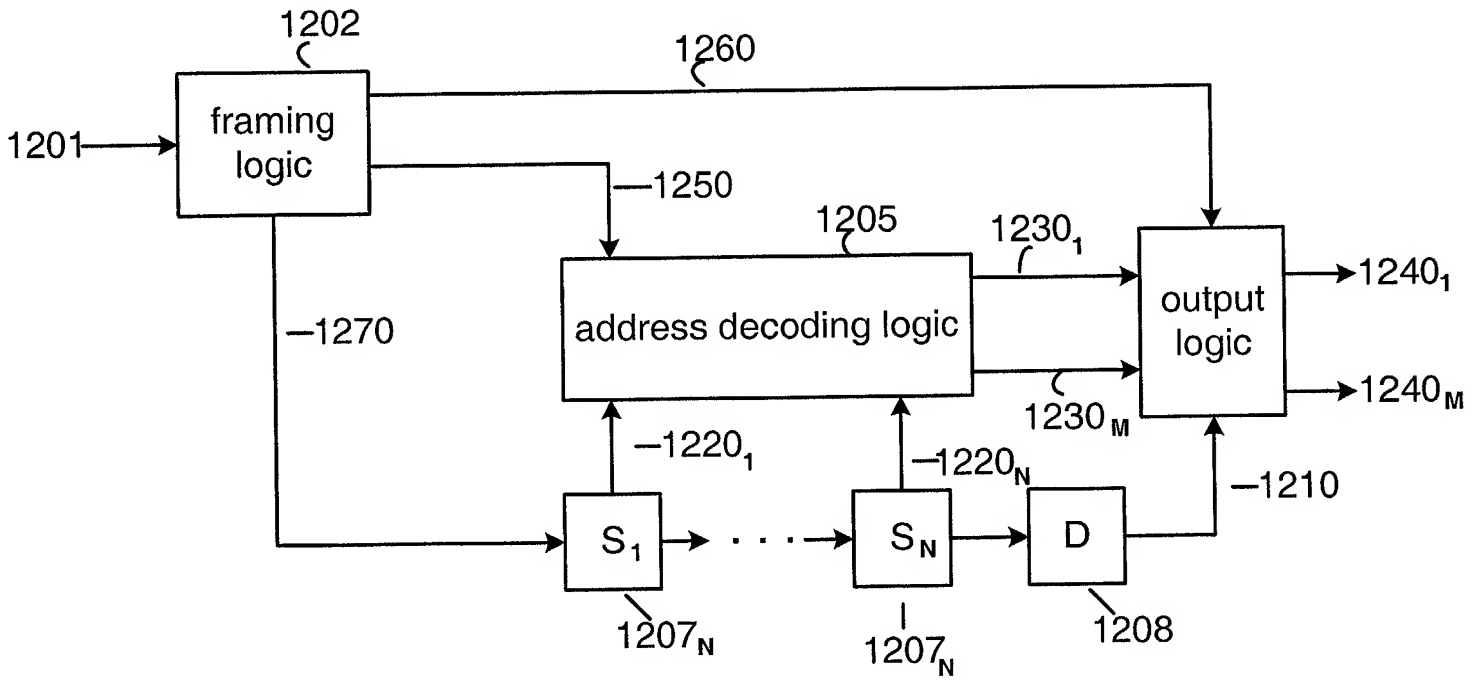
1202
1260
framing logic
1201
1250
1205
1230$_1$
address decoding logic
output logic
1240$_1$
1240$_M$
1270
1230$_M$
1220$_1$
1220$_N$
1210
S$_1$
S$_N$
D
1207$_N$
1207$_N$
1208

FIG. 37 3700

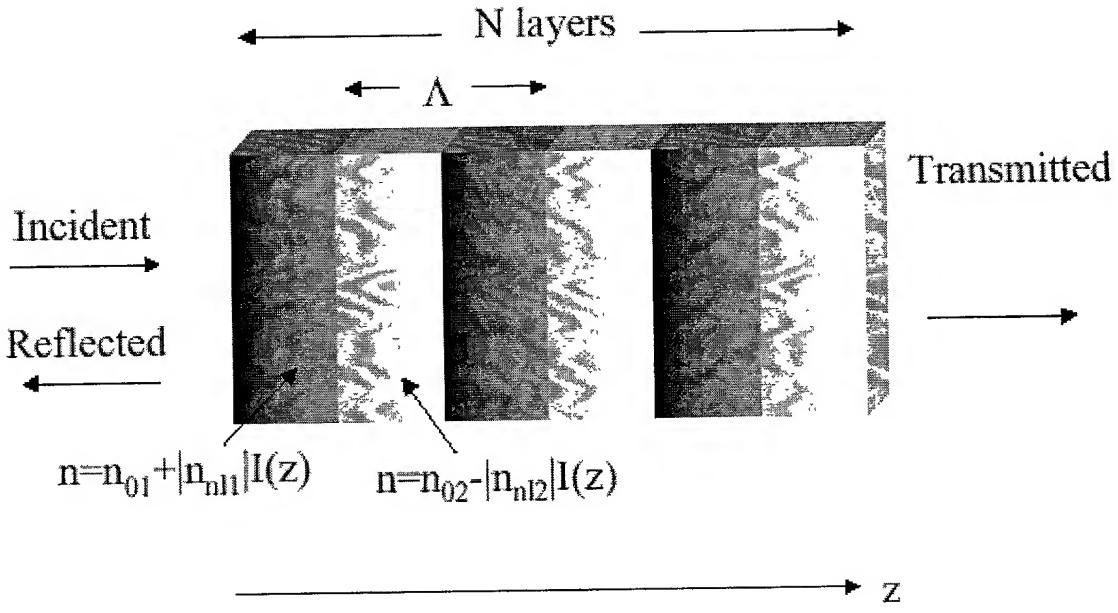
N layers
Λ
Incident
Reflected
Transmitted
$n=n_{01}+|n_{nl1}|I(z)$
$n=n_{02}-|n_{nl2}|I(z)$
z

FIG. 38

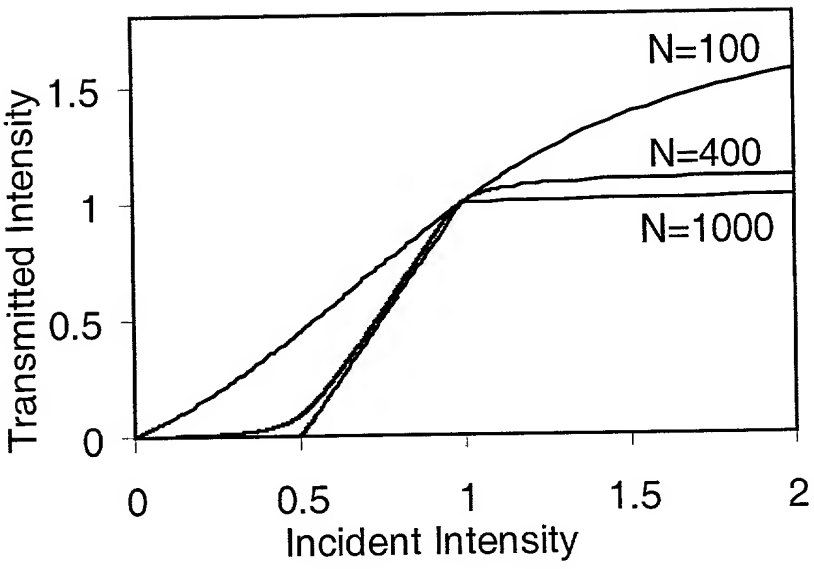
N=100
N=400
N=1000
Transmitted Intensity
1.5
1
0.5
0
0
0.5
1
1.5
2
Incident Intensity

FIG. 39

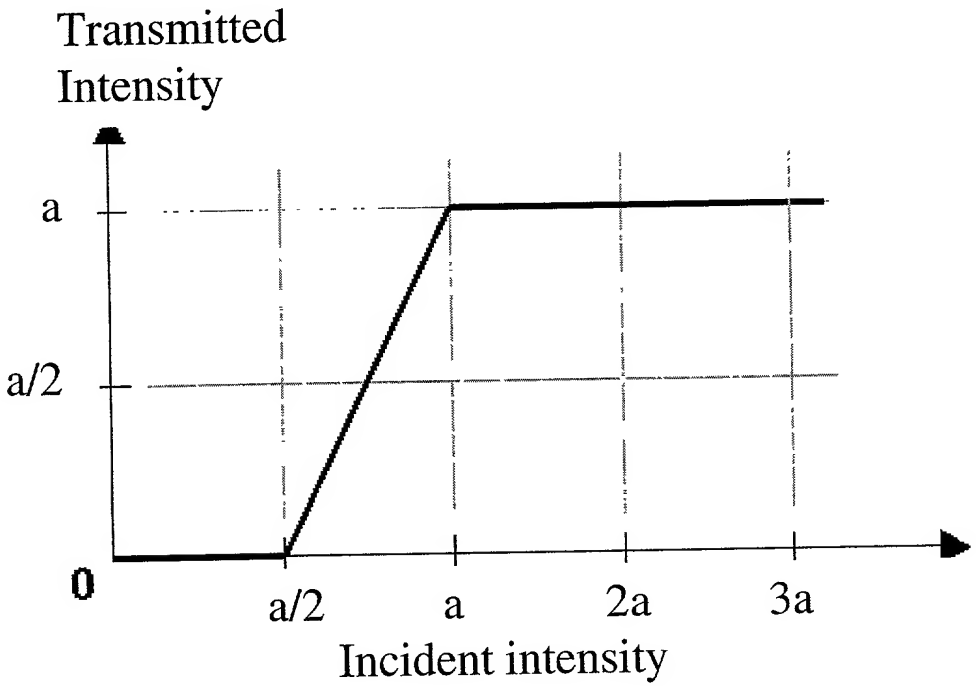

FIG. 40

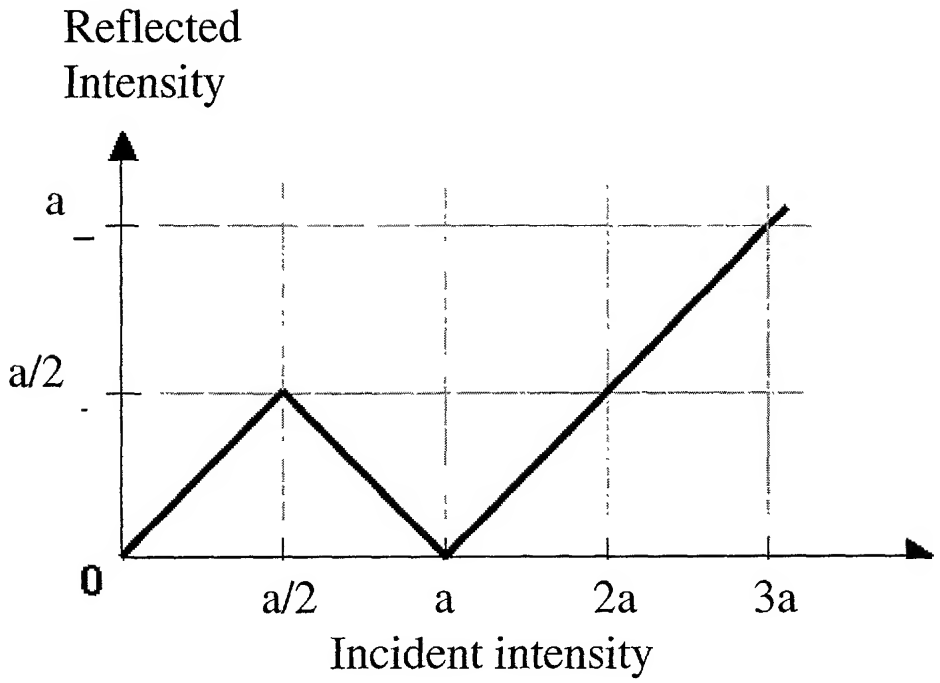

FIG. 41

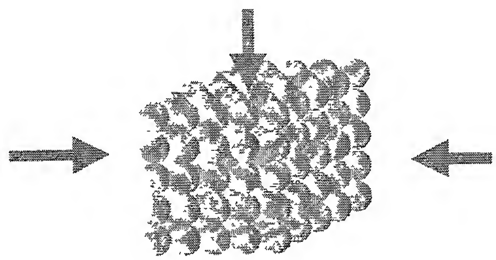

FIG. 42

FIG. 43

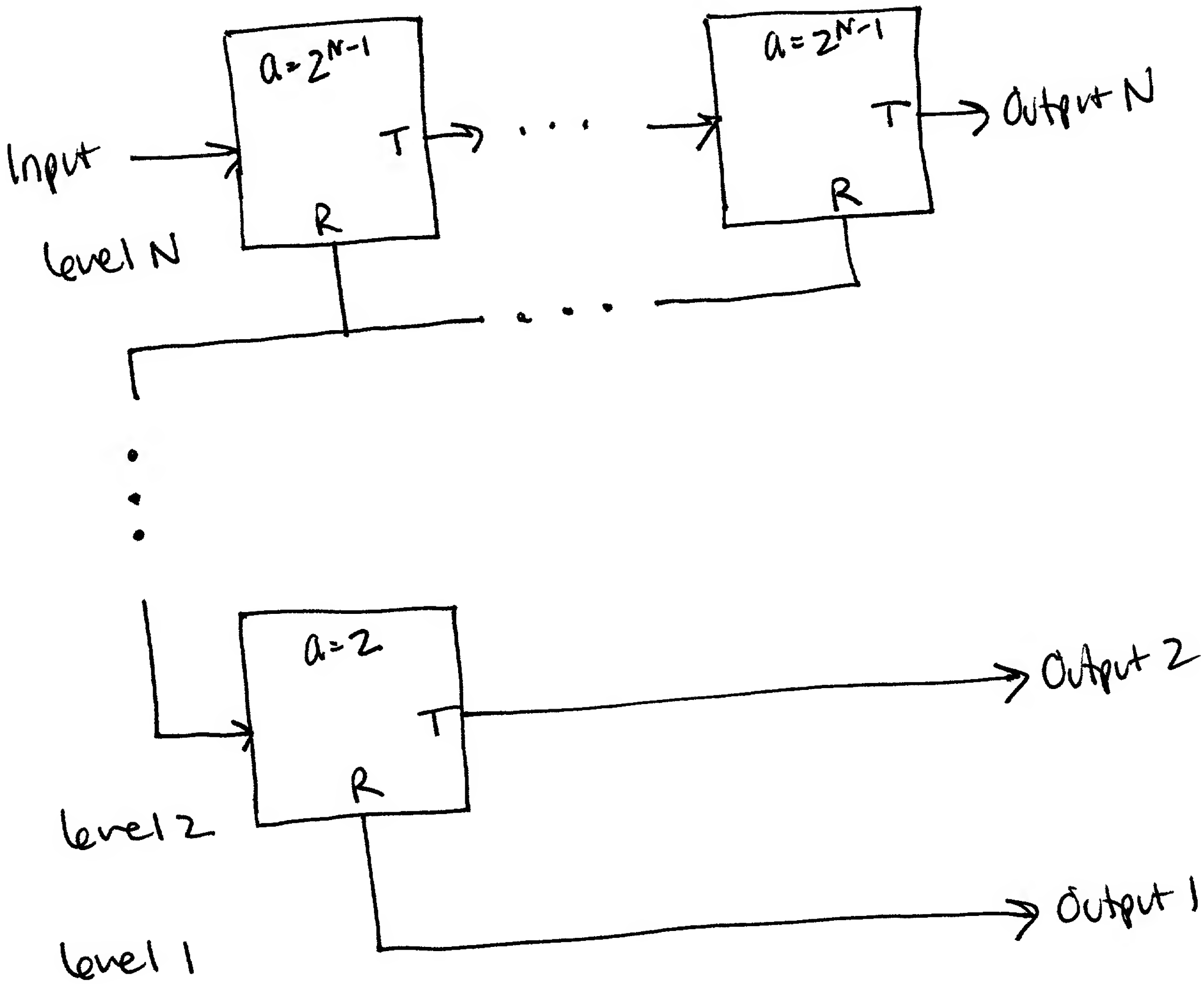
a=2^N-1
a=2^N-1
Input
T
T
Output N
R
R
level N
a=2
Output 2
T
R
level 2
Output 1
level 1

FIG. 44 4400

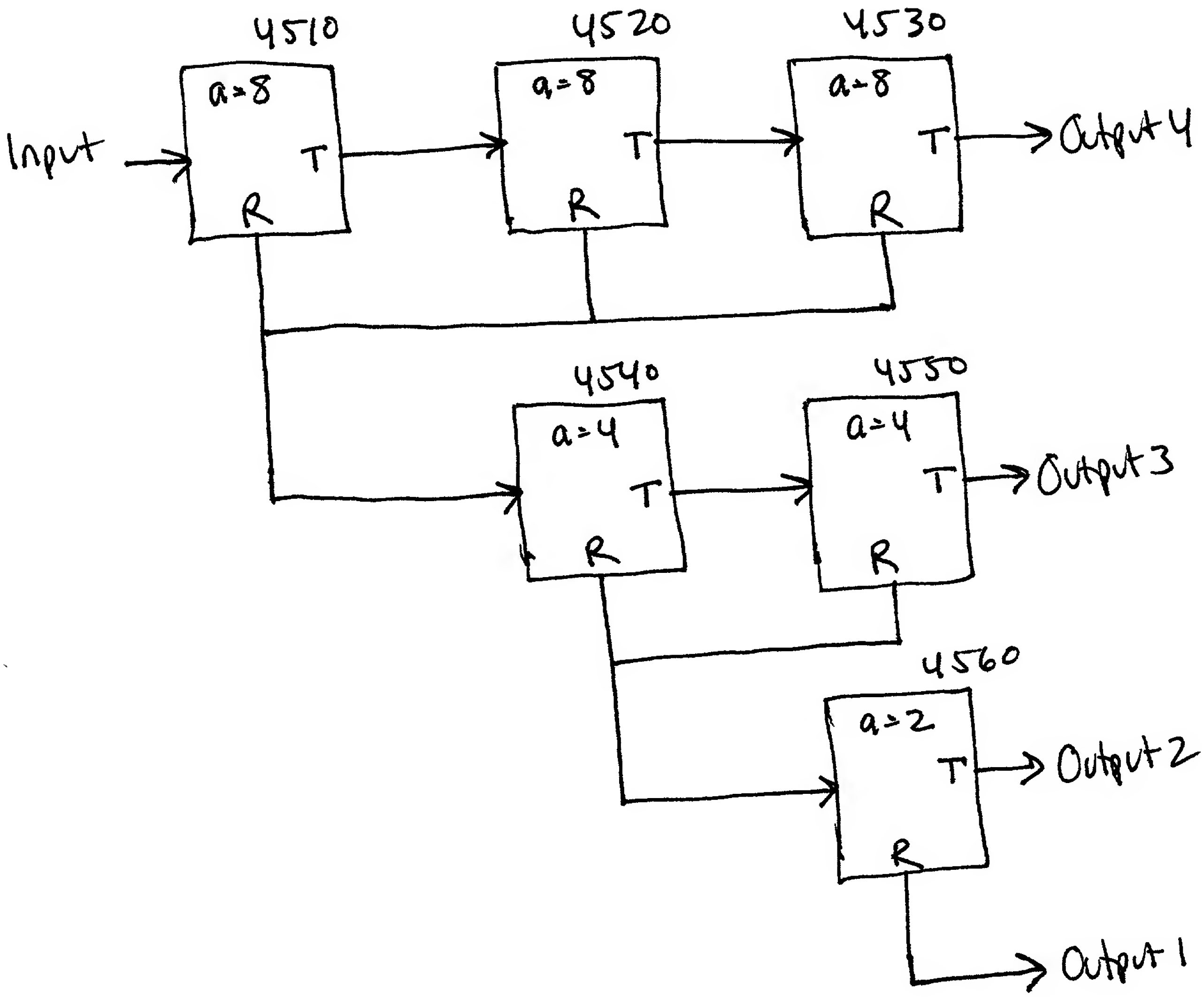

FIG. 45 4500

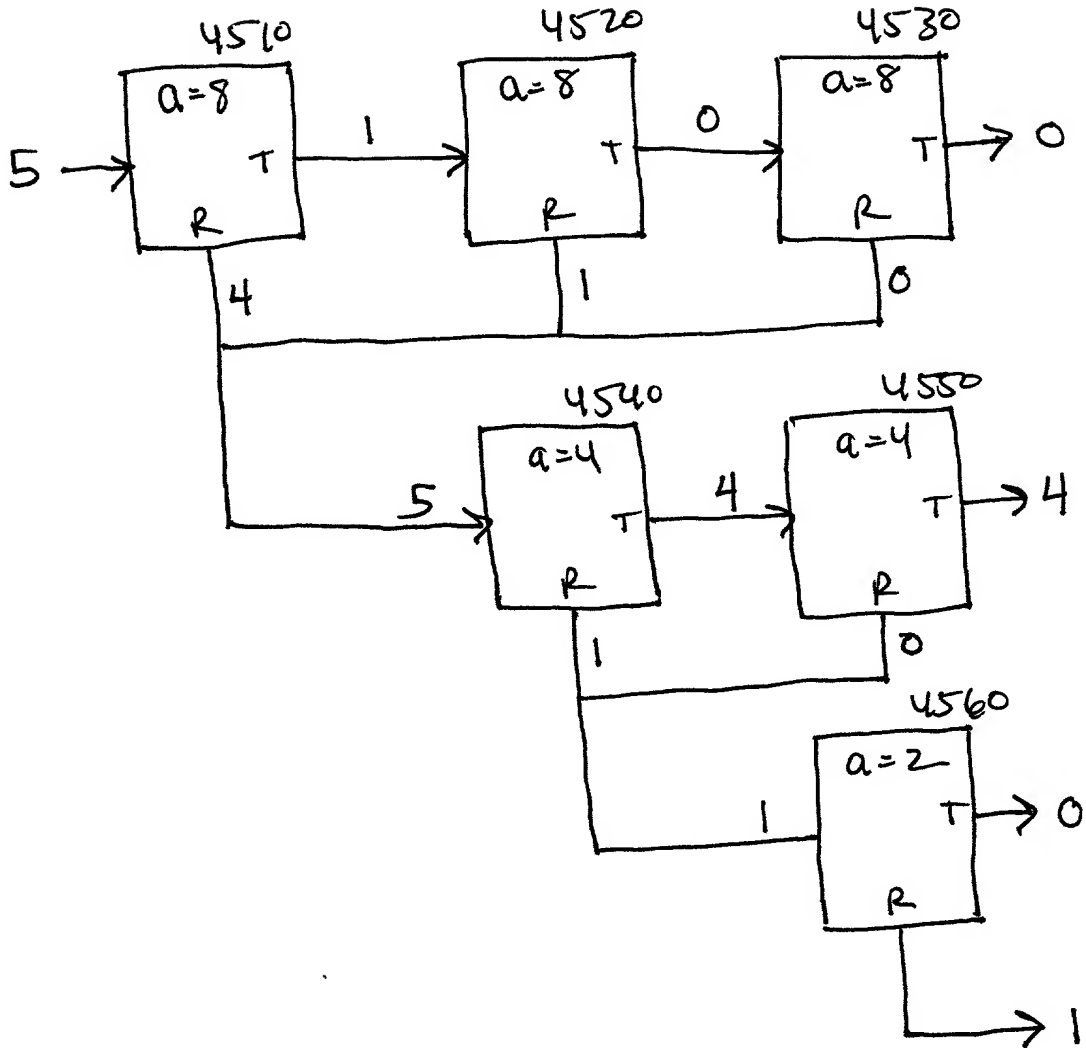

FIG. 46